Amendments to the Specification

Please replace the paragraph on page 2, lines 15-22 with the following amended paragraph:

In a source synchronous interface, a transmit clock signal from a link layer operates as a reference clock for all signals transmitted from the link layer to the PHY layer. A receive clock signal from the PHY layer operates as a reference clock for all the signals transmitted from the PHY layer to the link layer. As a result, receive flow control signals that originate from the link layer ~~is~~ are re-synchronized to the transmit clock before transmission to the PHY layer. Similarly, transmit control signals that originate from PHY layer ~~is~~ are re-synchronized to the receive clock prior to the transmission to the link layer.

Please replace the paragraph on page 6, lines 18-22 with the following amended paragraph:

The transmit clock 29 is delayed by the delay buffer 19 so that the transmit clock 29 is synchronized with the transmit data 28 when the transmit data ~~29~~ 28 exits from the transmit clock domain 4 onto the line 10. The buffer 22 in the transmit clock domain 5 is optional. The register 21 receives the transmit data 28 from the line 10 and has a second input for receiving the clock signal from the output of the buffer 23.

Please replace the paragraph on page 7, lines 1-8 with the following amended paragraph:

Optionally, the clock output from the buffer ~~23~~ 22 from the transmit clock domain 5 can be connected to with a receive clock 33 of the receive clock domain 6. As a result, the requirement of synchronizing the transmit data 29 with the receive data 33 is eliminated since the same clock is used for both the transmit data 29 in the transmit block domain 5 and the receive data 33 in the receive clock domain 6. The merging of the transmit clock 29 and the receive clock 33 ensure that the number of clock cycles on the transmit side match those on the receive side for receive flow control 11 and transmit flow control 17.